CLAIMS

What is claimed is:

1. An electronic device comprising:

a hard mask layer that is applied in a liquid phase to a line dielectric layer, wherein the hard mask layer comprises a Si-N bond, and wherein the hard mask layer is densified such that the hard mask has an etch resistivity that is greater than both an etch resistivity of the line dielectric layer and an etch resistivity of a via dielectric layer; and

wherein the hard mask layer, the line dielectric layer, the via dielectric layer, and a copper element are configured to form a dual damascene structure.

2. The electronic device of claim 1 wherein the line dielectric layer comprises an organic low dielectric constant material.

3. The electronic device of claim 2 wherein the organic low dielectric constant material is selected from the group consisting of a polyarylene ether, a polyarylene, a polyimide, and cyanate ester resin.

4. The electronic device of claim 1 wherein application of the hard mask in liquid phase comprises a spin-on process.

5. The electronic device of claim 1 wherein the hard mask layer is formed from a polyperhydrosilazane.

6. The electronic device of claim 5 wherein the polyperhydrosilazane has a structure represented by $(SiH_2\text{-}NH)_n$, wherein n is an integer between 2 and 2000.

7. The electronic device of claim 1 wherein the hard mask layer is densified using a process selected from the group consisting of a furnace cure process, a rapid thermal anneal process, a hot plate anneal process, and an electron beam process.

8. The electronic device of claim 1 further comprising a diffusion barrier, wherein the diffusion barrier is applied in a liquid phase to the hard mask layer, and wherein the diffusion barrier comprises a Si-N bond.

9. The electronic device of claim 8 wherein the diffusion barrier comprises a Si-N bond.

10. The electronic device of claim 9 wherein the diffusion barrier layer is formed from a polyperhydrosilazane.

11. The electronic device of claim 10 wherein the polyperhydrosilazane has a structure represented by $(SiH_2\text{-}NH)_n$, wherein n is an integer between 2 and 2000.

12. A method of forming a dual damascene structure, comprising:

providing a surface and depositing a low dielectric constant material onto the surface to form a first layer;

applying an etch stop layer in a liquid phase to the first layer, wherein the etch stop layer comprises a material including a Si-N bond; and

densifying the etch stop layer using a process selected from the group consisting of a furnace cure process, a rapid thermal anneal process, a hot plate anneal process, and an electron beam process.

13. The method of claim 12 further comprising applying a diffusion barrier layer in a liquid phase to the densified etch stop layer, wherein the diffusion barrier layer comprises a material including a Si-N bond.

14. The method of claim 13 wherein the dual damascene structure further includes copper as a conductive material.

15. The method of claim 12 wherein the low dielectric constant material comprises an organic low dielectric constant material.

16. The method of claim 15 wherein the organic low dielectric constant material is selected from the group consisting of a polyarylene ether, a polyarylene, a polyimide, and cyanate ester resin.

17. The method of claim 13 wherein the diffusion barrier layer material is a polysilazane or a polyperhydrosilazane.

18. The method of claim 17 wherein the polyperhydrosilazane has a structure represented by $(SiH_2\text{-}NH)_n$, wherein n is an integer between 2 and 2000.

19. The method of claim 13 wherein the step of densifying the etch stop layer uses an electron beam process.

20. The method of claim 13 wherein the etch stop layer and the diffusion barrier layer are formed from polyperhydrosilazane